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Title:

METHOD FOR MANUFACTURING A FLOATING GATE OF A DUAL GATE OF A SEMICONDUCTOR DEVICE

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METHOD FOR MANUFACTURING A FLOATING GATE OF A DUAL GATE OF A SEMICONDUCTOR DEVICE

BACKGROUND

Technical Field

A method for manufacturing a semiconductor device, which forms a floating gate in a dot shape before the formation of a dual gate of a semiconductor nonvolatile memory device.

Description of the Related Art

Generally, floating gates are used for storing charges to erase or delete data in memory devices of a nonvolatile metal oxide semiconductor (MOS) such as read only memories (ROM), erasable programmable read only memories (EPROM) and the like. One such conventional floating gate structure is shown in Fig. 1.

Fig. 1 is a cross sectional view for explaining a semiconductor device having a floating gate structure according to the prior art.

First, a tunnel oxide film layer 12, a floating gate oxide film layer 14, a control oxide film layer 16 and a control gate oxide film layer 18 are sequentially formed on a silicon substrate 10. Next, the control gate oxide film layer 18, the control oxide film layer 16, the floating gate oxide film layer 14, and the tunnel oxide film layer 12 are sequentially patterned into a predetermined shape by using a photographic process, thereby obtaining a floating gate structure shown in Fig. 1.

In order to form a thin film having the floating gate structure as shown in Fig. 1 and in order to collect electrons in the floating gate, a high voltage device is required. Further, in such a structure, even if only a single defective portion is generated in a tunnel oxide film 12, the electrons stored in the floating gate 14 all flow outward as leakage current thereby lowering the reliability of the device.

SUMMARY OF THE DISCLOSURE

In consideration of the above problems associated with the prior art structure of Fig. 1, a method for manufacturing a semiconductor device is disclosed, which can produce a low voltage device by forming a floating gate for a nonvolatile memory device comprising a continuous layer of discreet particles and determining a memory state by control of three to four electrons per particle, and which can improve the reliability of the device by restricting the leakage caused by a defective portion of a tunnel oxide film to only the floating gate particles on that portion.

A disclosed method for manufacturing a semiconductor device comprises: forming a tunnel oxide film on a silicon substrate where a predetermined substructure is formed; forming a particulate layer on the tunnel oxide film layer that serves as a floating gate layer; sequentially forming a control oxide film layer and a control gate layer on the particulate layer; and forming a dual gate by patterning the control gate layer, the control oxide film layer, the particulate floating gate layer and the tunnel oxide film layer into a predetermined shape.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects of the present disclosure will become apparent from the following description of embodiments with reference to the accompanying drawings, wherein:

Fig. 1 is a cross sectional view showing a dual gate structure formed according to the prior art;

Figs. 2 to 2e are cross sectional views showing a method for forming a dual gate structure according to a disclosed embodiment.

DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENT

Hereinafter, preferred embodiments will be described in greater detail in reference to the drawings. In addition, the following embodiments are for illustration only, not intended to limit the scope of this disclosure.

Figs. 2a to 2e are cross sectional views showing a method for manufacturing a semiconductor device according to this disclosure.

First, as shown in Fig. 2a, a tunnel oxide film layer 102 with a rough surface is formed on a silicon substrate 100 having a predetermined substructure. According to a preferred embodiment, the tunnel oxide film layer 102 is formed by depositing SiO_2, which is formed by diffusing oxygen, or a material having a high dielectric constant on the silicon substrate 100.

Then, as shown in Fig. 2b, a particulate layer or dots or a dotted layer composed of silicon or silicon-germanium are formed on the tunnel oxide film layer 102 for the floating gate layer 104 by chemical mechanical deposition (CVD) with a particle size of approximately less than 60 nm in diameter or cross-section at a density of about 10^{11} to 10^{12} dots or particles per cm^2 to form a particulate floating gate layer 104. In case of forming a particulate layer from silicon-germanium, it is preferred that the concentration of germanium ranges from about 10 to about 20%.

According to an embodiment, a thin film for a floating gate can be formed into the tunnel oxide film layer 102 by using Ta_2O_5, HfO_2, and ZrO_2, etc. having a high dielectric constant. And, before forming a floating gate oxide film, a metal layer comprising Ta, Hf, Zr, and etc. can be deposited. Further, the particulate layer floating gate 104 may be formed by using a rapid thermal CVD method.

In the next step, as shown in Figs. 2c and 2d, a control oxide film layer 106 and a control gate layer 108 are sequentially formed on the particulate floating gate layer 104. According to an embodiment, the control gate layer 108 is formed of a silicon-germanium thin film doped in-situ. Further, the control gate layer 108 can be formed of silicon or silicon-germanium.

Continuously, as shown in Fig. 2e, the tunnel oxide film layer 102, the particulate floating gate layer 104, the control oxide film layer 106 and the control gate layer 108 are sequentially patterned by an etching process such as lithography, thereby forming a dual gate provided with a floating gate 112, a dot floating gate 114, a control oxide film 116 and a control gate 118.

Furthermore, according to another embodiment, instead of formation by diffusing oxygen on a silicon substrate, a silicon oxide film is deposited by the CVD method, or an oxide film having a high dielectric constant such as Ta_2O_5, HfO_2, and ZrO_2, etc. is deposited by the CVD method. Next, a silicon or silicon-germanium compound is formed by the CVD method, and then can be formed into an oxide film such as Ta_2O_5, HfO_2, ZrO_2, etc., instead of a silicon oxide film, having a high dielectric constant and serving as a control oxide film.

As described above, by forming a floating gate in a particular layer 104 and inhibiting leakage current through the sides of the layer 104, the reliability of a device by preventing the degradation of the characteristics of the device due to only a single defective portion of the tunnel oxide film.

Furthermore, the present invention can provide low voltage device characteristics since three or four electrons per dot or particle enable a change in the memory state.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the sprit and scope of the appended claims.